

**PI3WVR31310A**

**DP/HDMI 1:3 De-mux/Mux Switches**

**Features**

- ➔ DP 1:3 De-Mux or 3:1 Mux switch with 4 high speed differential, AUX/DDC, HPD and CAB\_DET channels
- ➔ Pin selection for 1:3 DEMUX or 3:1 MUX
- ➔ HDMI 3:1 Mux switch with 4 high speed differential, DDC and HPD channels
- ➔ HDMI-mode only supports HDMI-sink application, not support HDMI-source application.
- ➔ Pin selection for DP mode or HDMI mode
- ➔ All ports support up to DP1.2 at 5.4Gb/s or HDMI 2.0 at 6Gb/s
- ➔ Supports manual switching or HPD auto priority selection in 1:3 DEMUX, in DP mode
- ➔ Low current consumption
- ➔ 3.3V power supply
- ➔ ESD protection on all I/O pins for 2kV HBM
- ➔ Package:  
60 pin TQFN (5x9mm)

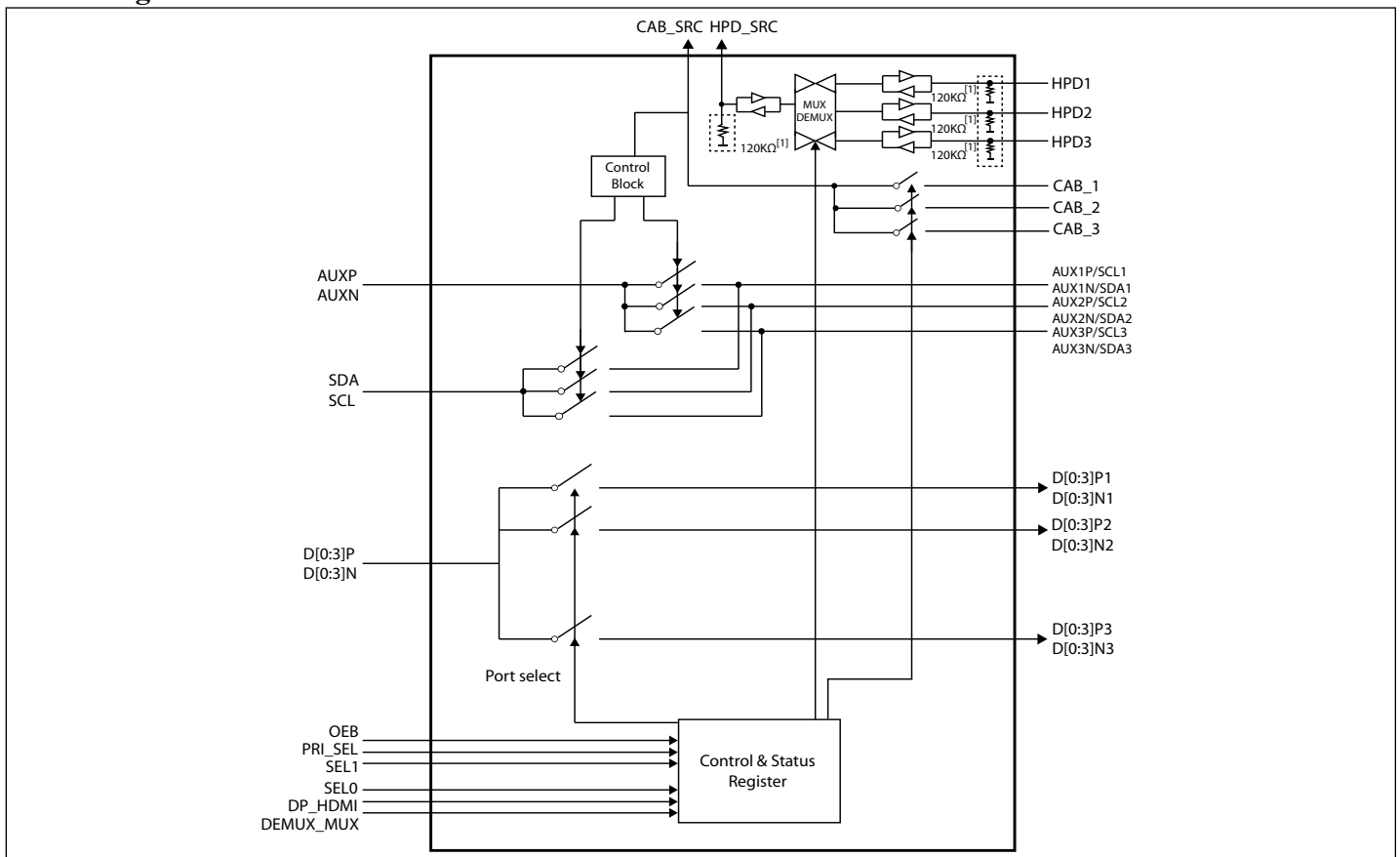
**Description**

The PI3WVR31310A is a 3:1 Mux or 1:3 Demux high speed passive switch supporting DP 1.2, HDMI 1.4, HDMI 2.0. At DEMUX mode, all three output ports support auto port priority selection by detecting HPD1/2/3 input or manual selection. At MUX mode, HPD1/2/3 will change from input to output, there is no auto port priority selection.

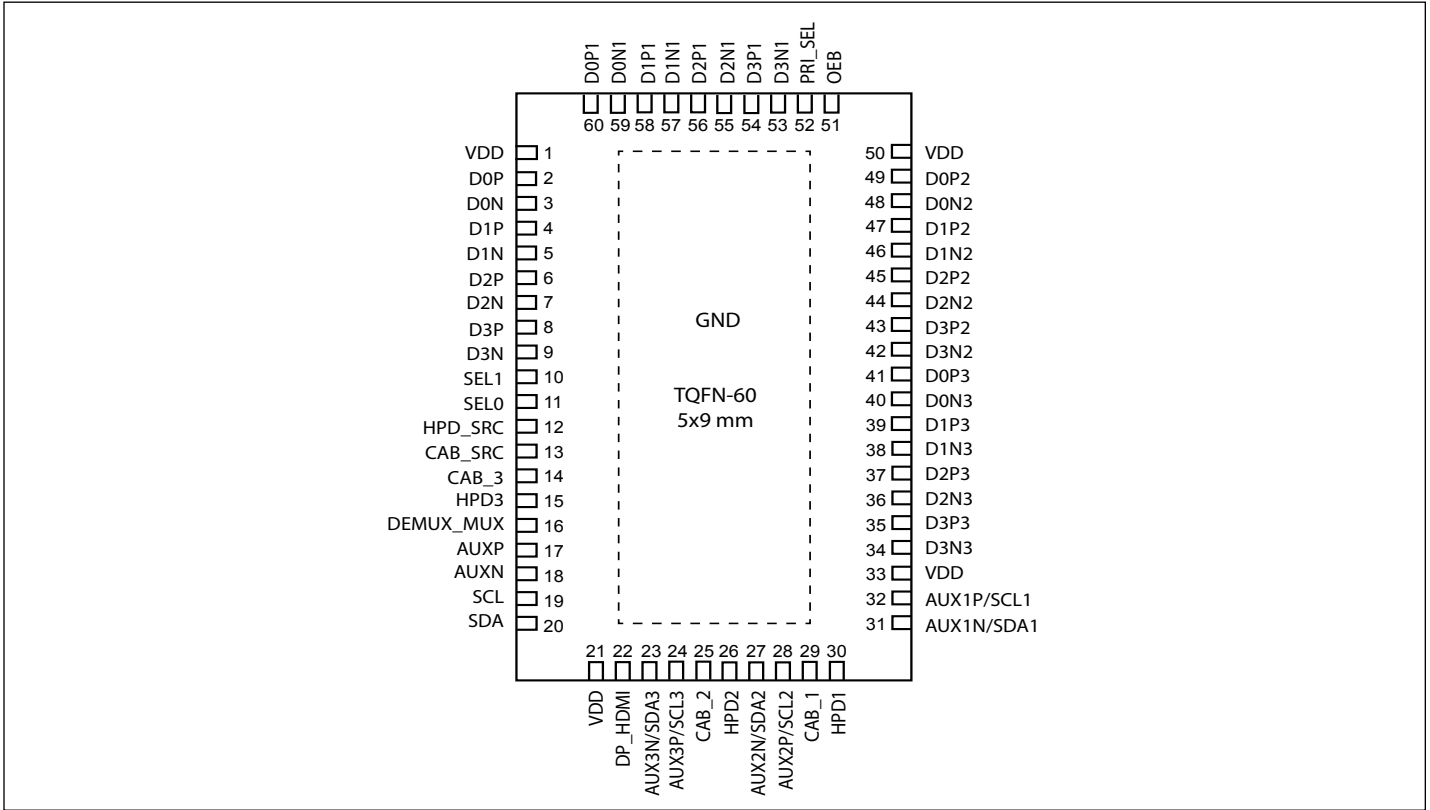
**Application**

- ➔ Notebook, Monitor, Switch box or TV sink application

**Block Diagram**



**Pin Configuration: TQFN-60**



**Note:** 1. The 120kΩ pull down resistor is not always on.

### Pin Description

| pin#  | pin Name  | Signal Type | Description                                     |
|---|---|-------------|---|
| 2,<br>4,<br>6,<br>8,<br>3,<br>5,<br>7,<br>9         | D0P,<br>D1P,<br>D2P,<br>D3P,<br>D0N,<br>D1N,<br>D2N,<br>D3N         | IO          | 4 differential pair I/O (DP or HDMI)            |
| 60,<br>58,<br>56,<br>54,<br>59,<br>57,<br>55,<br>53 | D0P1,<br>D1P1,<br>D2P1,<br>D3P1,<br>D0N1,<br>D1N1,<br>D2N1,<br>D3N1 | IO          | 4 differential pair I/O (DP or HDMI) for port 1 |
| 49,<br>47,<br>45,<br>43,<br>48,<br>46,<br>44,<br>42 | D0P2,<br>D1P2,<br>D2P2,<br>D3P2,<br>D0N2,<br>D1N2,<br>D2N2,<br>D3N2 | IO          | 4 differential pair I/O (DP or HDMI) for port 2 |
| 41,<br>39,<br>37,<br>35,<br>40,<br>38,<br>36,<br>34 | D0P3,<br>D1P3,<br>D2P3,<br>D3P3,<br>D0N3,<br>D1N3,<br>D2N3,<br>D3N3 | IO          | 4 differential pair I/O (DP or HDMI) for port 3 |

| pin#                                  | pin Name  | Signal Type | Description   |
|---------------------------------------|---|-------------|---|
| 31,<br>27,<br>23,<br>32,<br>28,<br>24 | AUX1N/SDA1,<br>AUX2N/SDA2,<br>AUX3N/SDA3,<br>AUX1P/SCL1,<br>AUX2P/SCL2,<br>AUX3P/SCL3 | IO          | AUX (DP) or DDC (HDMI) input from three ports   |
| 18,<br>17                             | AUXN,<br>AUXP   | IO          | AUX output  |
| 20,<br>19                             | SDA,<br>SCL   | IO          | DDC output  |
| 30,<br>26,<br>15,<br>12               | HPD1,<br>HPD2,<br>HPD3,<br>HPD_SRC  | IO          | When DEMUX_MUX = low (1:3 DEMUX mode), HPD1_2_3 are inputs, HPD_SRC is output;<br>When DEMUX_MUX = high (3:1 MUX mode), HPD1_2_3 are outputs, HPD_SRC is input                    |
| 29,<br>25,<br>14,<br>13               | CAB_1,<br>CAB_2,<br>CAB_3,<br>CAB_SRC   | IO          | CAB_1, CAB_2, CAB_3, CAB_SRC  |
| 51                                    | OEB   | I           | OEB=0, device active; OEB=1, device shut down   |
| 52                                    | PRI_SEL   | I           | PRI_SEL is for priority selection as in priority-selection-table, but only for 1:3 DEMUX mode. PRI_SEL has internal 100K divider between VDD and GND for middle-state with VDD/2. |
| 16                                    | DEMUX_MUX   | I           | DEMUX_MUX is for HPD direction selection, see truth table   |
| 22                                    | DP_HDMI   | I           | DP port or HDMI port, see truth table   |
| 11                                    | SEL0  | I           | Port selection pins, see truth table  |
| 10                                    | SEL1  | I           | Port selection pins, see truth table  |
| 1, 21, 33, 50                         | VDD   | Power       | 3.3V VDD  |
| Center Pad                            | GND   | Ground      | Bottom GND EPAD   |

### Pin mapping for dual mode DP source DEMUX to DP output

| DP mode    | HDMI/DVI mode | WVR31310A input pins | WVR31310A port1 output | WVR31310A port2 output | WVR31310A port3 output | DP mode    |
|------------|---------------|----------------------|------------------------|------------------------|------------------------|------------|
| ML_lan0(P) | TX2+          | D0P                  | D0P1                   | D0P2                   | D0P3                   | ML_lan0(P) |
| ML_lan0(N) | TX2-          | D0N                  | D0N1                   | D0N2                   | D0N3                   | ML_lan0(N) |
| ML_lan1(P) | TX1+          | D1P                  | D1P1                   | D1P2                   | D1P3                   | ML_lan1(P) |
| ML_lan1(N) | TX1-          | D1N                  | D1N1                   | D1N2                   | D1N3                   | ML_lan1(N) |
| ML_lan2(P) | TX0+          | D2P                  | D2P1                   | D2P2                   | D2P3                   | ML_lan2(P) |
| ML_lan2(N) | TX0-          | D2N                  | D2N1                   | D2N2                   | D2N3                   | ML_lan2(N) |
| ML_lan3(P) | TXC+          | D3P                  | D3P1                   | D3P2                   | D3P3                   | ML_lan3(P) |
| ML_lan3(N) | TXC-          | D3N                  | D3N1                   | D3N2                   | D3N3                   | ML_lan3(N) |

### Function Description

Default input format is DP. DP\_HDMI can select between DP or HDMI input.

In Demux mode, there are 120K pull down in HPD1/HPD2/HPD3 pins. In Mux mode, there is 120K pull down in HPD\_SRC pin.

Output port can be selected by manual or automatically in DEMUX mode.

Automatic port selection is done by detection of HPD presence from the output ports. If multiple HPD are detected, port selection depends on a priority scheme defined by PRI\_SEL pin. There can be 3 priority schemes. When PRI\_SEL=low, the port priority order is port1/port2/port3; when PRI\_SEL=high, the port priority order is port2/port3/port1; when PRI\_SEL=M (open), the port priority order is port3/port1/port2.

When port 1 or port 2 or port 3 is selected in DP application, and CAB=LOW, AUX/DDC input pins are now AUX channel. AUXP will have 100Kohm resistor to GND while AUXN will have 100Kohm resistor to VDD in external port side. Max. AUX data rate can be 720Mb/s. DDC switch inside is off.

When port 1 or port 2 or port 3 is active in dual mode DP or HDMI application, and CAB=HIGH, AUX/DDC input pins are now DDC channel. AUX switch inside is off, DDC switch is on. The DDC switch can support 5V input, and output Vpass is less than 3.3V limit.

HPD is CMOS buffer, and support 5v inputs. When used as DEMUX, There're 120kΩ pull-down resistors inside connected to HPD1, HPD2, HPD3 as input, and when used as MUX, 120k resistor connected to HPD\_SRC as input.

### Truth Table

DEMUX\_MUX

| DEMUX_MUX | HPD_SRC | HPD1/2/3 |
|-----------|---------|----------|
| 0 (DEMUX) | output  | input    |
| 1 (MUX)   | input   | output   |

DP\_HDMI

| DP_HDMI | Mode      |
|---------|-----------|
| 0       | DP Mode   |
| 1       | HDMI Mode |

SLE1/SEL0 in 1:3 DP modes

| SEL1 | SEL0 | PRI_SEL<br>(priority selection) | HPD/CAB_DET        | D[0:3]P, D[0:3]N, AUX/DDC |
|------|------|---------------------------------|--------------------|---------------------------|
| 0    | 0    | NC                              | HPD1/CAB_1         | Port 1                    |
| 0    | 1    | NC                              | HPD2/CAB_2         | Port 2                    |
| 1    | 0    | NC                              | HPD3/CAB_3         | Port 3                    |
| 1    | 1    | Auto-selection                  | See priority table | See priority table        |

SLE1/SEL0 in 3:1 HDMI mode and DP mode

| SEL1 | SEL0 | PRI_SEL<br>(priority selection) | HPD                | D[0:3]P, D[0:3]N, AUX/DDC |
|------|------|---------------------------------|--------------------|---------------------------|
| 0    | 0    | NC                              | HPD=HPD1, HPD2/3=0 | Port 1                    |
| 0    | 1    | NC                              | HPD=HPD2, HPD1/3=0 | Port 2                    |
| 1    | 0    | NC                              | HPD=HPD3, HPD1/2=0 | Port 3                    |
| 1    | 1    | NC                              | NC                 | NC                        |

AUX and DDC

| PORT                | DP_HDMI | CAB_1 | CAB_2 | CAB_3 | AUXP  | AUXN  | SCL  | SDA  |
|---------------------|---------|-------|-------|-------|-------|-------|------|------|
| When Port1 Selected | 0       | 0     | x     | x     | AUX1P | AUX1N | Hi-Z | Hi-Z |
|                     | 0       | 1     | x     | x     | Hi-Z  | Hi-Z  | SCL1 | SDA1 |
|                     | 1       | 1     | x     | x     | Hi-Z  | Hi-Z  | SCL1 | SDA1 |
| When Port2 Selected | 0       | x     | 0     | x     | AUX2P | AUX2N | Hi-Z | Hi-Z |
|                     | 0       | x     | 1     | x     | Hi-Z  | Hi-Z  | SCL2 | SDA2 |
|                     | 1       | x     | 1     | x     | Hi-Z  | Hi-Z  | SCL2 | SDA2 |
| When Port3 Selected | 0       | x     | x     | 0     | AUX3P | AUX3N | Hi-Z | Hi-Z |
|                     | 0       | x     | x     | 1     | Hi-Z  | Hi-Z  | SCL3 | SDA3 |
|                     | 1       | x     | x     | 1     | Hi-Z  | Hi-Z  | SCL3 | SDA3 |

**Priority Selection Table**

| PRI_SEL<br>(Priority order) | HPD1 | HPD2 | HPD3 | HPD_SRC | CAB_SRC | AUXP/AUXN   | SDA/SCL   |
|-----------------------------|------|------|------|---------|---------|-------------|-----------|
| 0                           | 0    | 0    | 0    | 0       | Hi-Z    | Hi-Z        | Hi-Z      |
| 0                           | 1    | x    | x    | HPD1    | CAB1    | AUX1P/AUX1N | SDA1/SCL1 |
| 0                           | 0    | 1    | x    | HPD2    | CAB2    | AUX2P/AUX2N | SDA2/SCL2 |
| 0                           | 0    | 0    | 1    | HPD3    | CAB3    | AUX3P/AUX3N | SDA3/SCL3 |
| M                           | 0    | 0    | 0    | 0       | Hi-Z    | Hi-Z        | Hi-Z      |
| M                           | 1    | x    | 0    | HPD1    | CAB1    | AUX1P/AUX1N | SDA1/SCL1 |
| M                           | 0    | 1    | 0    | HPD2    | CAB2    | AUX2P/AUX2N | SDA2/SCL2 |
| M                           | x    | x    | 1    | HPD3    | CAB3    | AUX3P/AUX3N | SDA3/SCL3 |
| 1                           | 0    | 0    | 0    | 0       | Hi-Z    | Hi-Z        | Hi-Z      |
| 1                           | 1    | 0    | 0    | HPD1    | CAB1    | AUX1P/AUX1N | SDA1/SCL1 |
| 1                           | x    | 1    | x    | HPD2    | CAB2    | AUX2P/AUX2N | SDA2/SCL2 |
| 1                           | x    | 0    | 1    | HPD3    | CAB3    | AUX3P/AUX3N | SDA3/SCL3 |

Note: M= VDD/2 or open (with internal VDD/2)

| PRI_SEL<br>(Priority order) | HPD1 | HPD2 | HPD3 | D0P  | D1P  | D2P  | D3P  | D0N  | D1N  | D2N  | D3N  |
|-----------------------------|------|------|------|------|------|------|------|------|------|------|------|
| 0                           | 0    | 0    | 0    | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| 0                           | 1    | x    | x    | D0P1 | D1P1 | D2P1 | D3P1 | D0N1 | D1N1 | D2N1 | D3N1 |
| 0                           | 0    | 1    | x    | D0P2 | D1P2 | D2P2 | D3P2 | D0N2 | D1N2 | D2N2 | D3N2 |
| 0                           | 0    | 0    | 1    | D0P3 | D1P3 | D2P3 | D3P3 | D0N3 | D1N3 | D2N3 | D3P3 |
| M                           | 0    | 0    | 0    | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| M                           | 1    | x    | 0    | D0P1 | D1P1 | D2P1 | D3P1 | D0N1 | D1N1 | D2N1 | D3N1 |
| M                           | 0    | 1    | 0    | D0P2 | D1P2 | D2P2 | D3P2 | D0N2 | D1N2 | D2N2 | D3N2 |
| M                           | x    | x    | 1    | D0P3 | D1P3 | D2P3 | D3P3 | D0N3 | D1N3 | D2N3 | D3P3 |
| 1                           | 0    | 0    | 0    | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| 1                           | 1    | 0    | 0    | D0P1 | D1P1 | D2P1 | D3P1 | D0N1 | D1N1 | D2N1 | D3N1 |
| 1                           | x    | 1    | x    | D0P2 | D1P2 | D2P2 | D3P2 | D0N2 | D1N2 | D2N2 | D3N2 |
| 1                           | x    | 0    | 1    | D0P3 | D1P3 | D2P3 | D3P3 | D0N3 | D1N3 | D2N3 | D3P3 |

Note: M= VDD/2 or open (with internal VDD/2)

Note: For priority selection control, when PRI\_SEL = 0, the order is port1/port2/port3; when PRI\_SEL = 1, the order is port2/port3/port1; when PRI\_SEL = M, the order is port3/port1/port2.

## Maximum Ratings

(Above which useful life may be impaired. For user guidelines not tested.)

|  |                 |  |
|--|-----------------|--|
| Storage Temperature .....                          | -65°C to +150°C | <b>Note:</b> Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. |
| Supply Voltage to Ground Potential .....           | -0.5V to +4.6V  |  |
| High Speed Channel Input Voltage (DP Mode).....    | -0.5V to 2V     |  |
| High Speed Channel Input Voltage (HDMI Mode) ..... | 2.4V to 3.6V    |  |
| DDC and HPD channels Input Voltage .....           | -0.5V to 6V     |  |
| DC Output Current .....                            | 40mA            |  |
| Power Dissipation .....                            | 0.2W            |  |

## Electrical Characteristics

### Recommended Operation Conditions

$V_{DD} = 3.3V \pm 10\%$ , Min and Max apply for  $T_A$  between  $-40^\circ C$  to  $85^\circ C$  Typical values are referenced to  $T_A = 25^\circ C$

| Parameter | Description                               | Test Conditions                       | Min. | Typ. | Max. | Unit |
|-----------|---|---------------------------------------|------|------|------|------|
| $V_{DD}$  | Operating Voltage                         |                                       | 3.0  | 3.3  | 3.6  | V    |
| $I_{DD}$  | VDD supply current                        | $V_{DD}=3.3V$                         |      | 1    |      | mA   |
| Istd      | Supply current when OEB disable HDMI Mode | $V_{DD}=3.6V$ , OEB=high<br>DP_HDMI=1 |      | 0.7  |      | mA   |
|           | Supply current when OEB disable DP Mode   | $V_{DD}=3.6V$ , OEB=high<br>DP_HDMI=0 |      | 10   |      | uA   |

### DC Electrical Characteristics for Switching over Operating Range

| Parameter              | Description                         | Test Conditions   | Min.   | Typ. | Max.   | Unit       |
|------------------------|-------------------------------------|-------------------|--------|------|--------|------------|
| <b>OEB, SEL1, SEL0</b> |                                     |                   |        |      |        |            |
| $I_{IH}$               | High level digital input current    | $V_{IH} = V_{DD}$ | -10    |      | 40     | $\mu A$    |
| $I_{IL}$               | Low level digital input current     | $V_{IL} = GND$    | -10    |      | 10     | $\mu A$    |
| $V_{IH}$               | High level digital input voltage    |                   | 2.0    |      |        | V          |
| $V_{IL}$               | Low level digital input voltage     |                   | 0      |      | 0.8    | V          |
| <b>DEMUX_MUX</b>       |                                     |                   |        |      |        |            |
| $I_{IH}$               | High level digital input current    | $V_{IH} = V_{DD}$ | -10    |      | 40     | $\mu A$    |
| $I_{IL}$               | Low level digital input current     | $V_{IL} = GND$    | -10    |      | 10     | $\mu A$    |
| $V_{IH}$               | High level digital input voltage    |                   | 2.7    |      |        | V          |
| $V_{IL}$               | Low level digital input voltage     |                   | 0      |      | 0.8    | V          |
| <b>DP_HDMI</b>         |                                     |                   |        |      |        |            |
| $R_{pd}$               | Inter Pull-down resistor on DP_HDMI |                   |        | 100  |        | k $\Omega$ |
| $V_{IH}$               | High level digital input voltage    |                   | 0.7Vdd |      |        | V          |
| $V_{IL}$               | Low level digital input voltage     |                   | 0      |      | 0.3Vdd | V          |



| Parameter  | Description   | Test Conditions  | Min. | Typ. | Max. | Unit |
|--|---|--|------|------|------|------|
| <b>HPD_SRC (when HPD_SRC is output, HPD 1, 2, 3 are inputs)</b>          |   |  |      |      |      |      |
| V <sub>IH</sub>  | High level digital input voltage                    | V <sub>DD</sub> =3.3V  | 2.0  |      |      | V    |
| V <sub>IL</sub>  | Low level digital input voltage                     | V <sub>DD</sub> =3.3V  | 0    |      | 0.8  | V    |
| V <sub>OL</sub> _HPD_SRC   | Buffer Output Low Voltage                           | I <sub>OL</sub> = 4 mA   |      |      | 0.4  | V    |
| V <sub>OH</sub> _HPD_SRC   | Buffer Output Low Voltage                           | I <sub>OH</sub> = 4 mA   | 2.4  |      |      | V    |
| <b>HPD_Sink (when HPD_SRC is input, HPD 1, 2, 3 are as sink outputs)</b> |   |  |      |      |      |      |
| V <sub>IH</sub>  | High level digital input voltage                    | V <sub>DD</sub> =3.3V  | 2.0  |      |      | V    |
| V <sub>IL</sub>  | Low level digital input voltage                     |  | 0    |      | 0.8  | V    |
| V <sub>OL</sub> _HPD_Sink  | Buffer Output Low Voltage                           | I <sub>OL</sub> = 4 mA   |      |      | 0.4  | V    |
| V <sub>OH</sub> _HPD_Sink  | Buffer Output Low Voltage                           | I <sub>OH</sub> = 4 mA   | 2.4  |      |      | V    |
| <b>CAB</b>   |   |  |      |      |      |      |
| I <sub>LK</sub>  | Input leakage current                               | Switch is off, V <sub>in</sub> =5.5V                                 | -50  |      | 50   | uA   |
| C <sub>IO</sub>  | Input/Output capacitance when passive switch on     |  |      | 10   |      | pF   |
| R <sub>ON</sub>  | Passive Switch resistance                           | I <sub>O</sub> = 3mA, V <sub>O</sub> = 0.4V                          |      | 25   | 50   | Ω    |
| V <sub>pass</sub>  | Switch Output voltage                               | V <sub>I</sub> =3.3V, I <sub>I</sub> =100uA                          | 3.0  | 3.5  | 4.0  | V    |
| CI(source)   | Source side CAB capacitance                         | V <sub>I</sub> peak-peak = 1V, 100 KHz                               |      | 3.5  |      | pF   |
| CI(sink)   | Sink side CAB capacitance when                      |  |      | 6.5  |      | pF   |
| <b>SDA/SCL, SDA1/SCL1, SDA2/SCL2, SDA3/SCL3 (passive switch)</b>         |   |  |      |      |      |      |
| I <sub>LK</sub>  | Input leakage current                               | DDC switch is off, V <sub>in</sub> =5.5V                             | -50  |      | 50   | uA   |
| C <sub>IO</sub>  | Input/Output capacitance when passive switch on     | V <sub>I</sub> peak-peak = 1V, 100 KHz                               |      | 10   |      | pF   |
| R <sub>ON</sub>  | Passive Switch resistance                           | I <sub>O</sub> = 3mA, V <sub>O</sub> = 0.4V                          |      | 25   | 50   | Ω    |
| V <sub>pass</sub>  | Switch Output voltage                               | V <sub>I</sub> =5.0V, I <sub>I</sub> =100uA<br>V <sub>DD</sub> =3.3V | 1.5  | 2.0  | 2.5  | V    |
| CI(source)   | Source side DDC capacitance ( passive switch off. ) | V <sub>I</sub> peak-peak = 1V, 100 KHz                               |      | 2.5  |      | pF   |
| CI(sink)   | Sink side DDC capacitance ( passive switch off. )   | V <sub>I</sub> peak-peak = 1V, 100 KHz                               |      | 9    |      | pF   |
| <b>AUXP, AUXN, AUXnP/SCLn, AUXnN/SDAn</b>                                |   |  |      |      |      |      |
| I <sub>LK</sub>  | Input leakage current                               | DDC switch is off, V <sub>in</sub> =5.5V                             | -50  |      | 50   | uA   |
| C <sub>IO</sub>  | Input/Output capacitance when passive switch on     | V <sub>I</sub> peak-peak = 1V, 100 KHz                               |      | 7    |      | pF   |
| R <sub>ON</sub>  | Passive Switch resistance                           | I <sub>O</sub> = 3mA, V <sub>O</sub> = 0.4V                          |      | 5    | 15   | Ω    |
| V <sub>pass</sub>  | Switch Output voltage                               | V <sub>I</sub> =5.5V, I <sub>I</sub> =100uA<br>V <sub>DD</sub> =3.3V | 3.0  | 4.0  | 4.5  | V    |
| CI(source)   | Source side capacitance ( passive switch off. )     | V <sub>I</sub> peak-peak = 1V, 100 KHz                               |      | 2.5  |      | pF   |

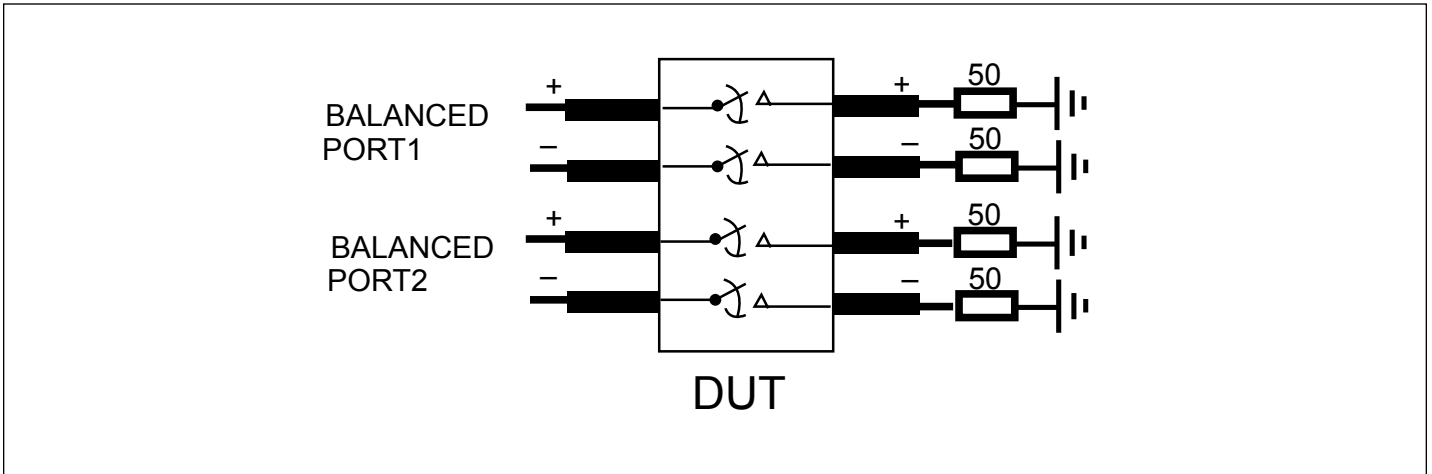
|                     |
|---------------------|
| <b>PI3WVR31310A</b> |
|---------------------|

| Parameter  | Description  | Test Conditions  | Min. | Typ. | Max.     | Unit          |
|--|--|--|------|------|----------|---------------|
| CI(sink)   | Sink side capacitance ( passive switch off. )                  | $V_I$ peak-peak = 1V, 100 KHz  |      | 3.5  |          | pF            |
| <b>High Speed Channel (D[0:3]P/N – D[0:3]P1N1, D[0:3]P/N – D[0:3]P2N2)</b> |  |  |      |      |          |               |
| $V_{IK}$   | Clamp Diode Voltage (HS Channel)                               | $V_{DD} = \text{Max.}, I_{IN} = -18\text{mA}$  |      | -1.6 | -1.8     | V             |
| $I_{IH}$   | Input HIGH Current   | $V_{DD} = \text{Max.}, V_{IN} = V_{DD}$  |      |      | $\pm 10$ | $\mu\text{A}$ |
| $I_{IL}$   | Input LOW Current  | $V_{DD} = \text{Max.}, V_{IN} = \text{GND}$  |      |      | $\pm 10$ |               |
| $R_{ON\_HS}$   | On resistance between input to out- put for high speed signals | $V_{INPUT,cm} = 0\text{V to } 0.8\text{V},$<br>$V_{INPUT,diff} < 1.0V_{p-p,diff}$<br>$V_{DD} = 3.0\text{V}, I_{INPUT} = 20\text{mA}$   |      | 8    | 12       | Ohm           |
|  |  | $V_{INPUT,cm} = 2.2\text{V to } 3.1\text{V},$<br>$V_{INPUT,diff} < 1.2V_{p-p,diff}$<br>$V_{DD} = 3.0\text{V}, I_{INPUT} = 20\text{mA}$ |      | 8    | 12       | Ohm           |
| Input signal voltage range   | HDMI MUX mode  | Channel on   | 2.4  |      | 3.3      | V             |
|  | HDMI MUX mode  | Channel off  | 0    |      | 3.3      | V             |

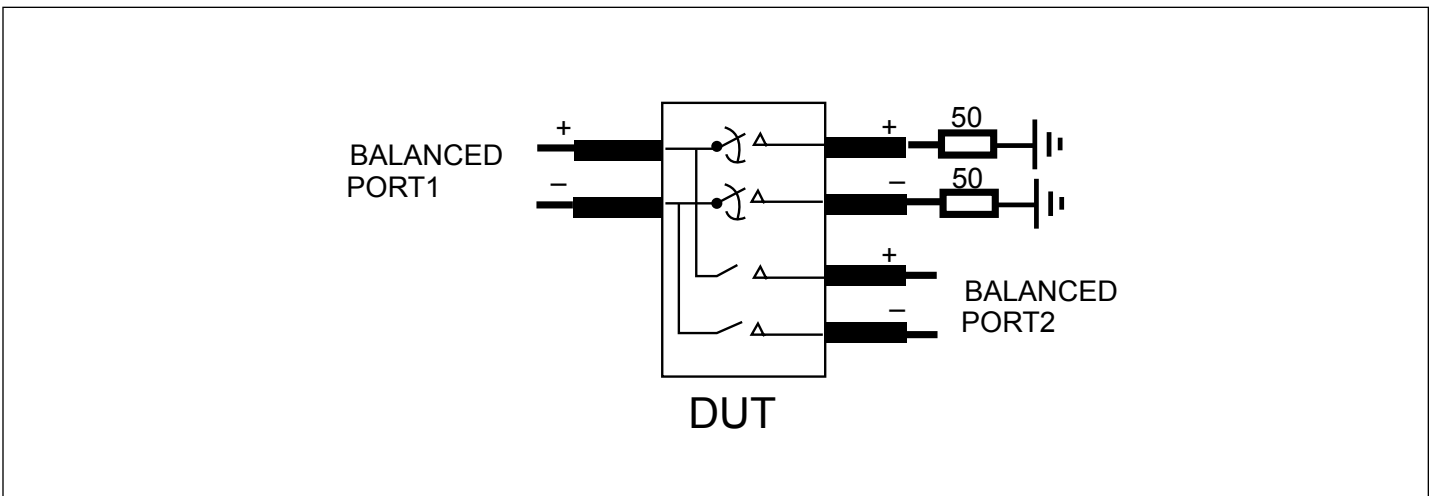
**Note:** High speed channel does not support Ioff when  $V_{DD}=0$

## Dynamic Electrical Characteristics

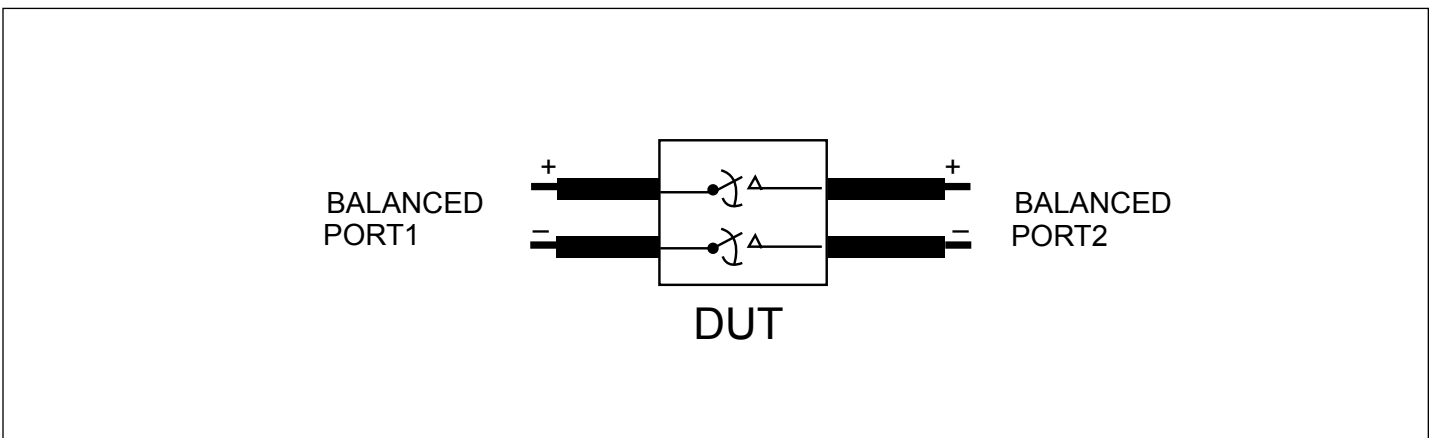
| Parameter  | Description  | Test Conditions  | Min.        | Typ. <sup>(1)</sup> | Max. | Unit |
|--|--|--|-------------|---------------------|------|------|
| <b>SCL, SDA channel, AUX channel, CAB channel (passive switch)</b> |  |  |             |                     |      |      |
| t <sub>pd</sub> (DDC)  | Propagation delay from SCLn/SDAn to SCL/SDA or SCL/SDA to SCLn/SDAn<br>In passive SW on. | C <sub>L</sub> = 10pF, in passive switch                                       |             |                     | 5    | ns   |
|  |  | C <sub>L</sub> = 10pF, in active switch<br>(1.5k to 5k pull high, 10pf to GND) |             |                     | 60   |      |
| <b>Control and Status Pins (HPDn, HPD_SRC)</b>                     |  |  |             |                     |      |      |
| t <sub>pd</sub> (HPD)  | Propagation delay (from HPDx to the active port of HPD_SRC, high to low)                 | C <sub>L</sub> = 10pF, manual selection mode; auto mode refer to auto timing   |             | 10                  |      | ns   |
| tsx(HPD)   | Switch time (from port select to the latest HPD )  |  |             | 5                   |      | us   |
| X <sub>TALK</sub>  | Crosstalk on High Speed Channels   | See Fig.1 for Measurement Setup  | f = 2.7 GHz | -26                 | -23  | dB   |
|  |  |  | f = 3.0 GHz | -24                 | -21  |      |
| O <sub>IRR</sub>   | OFF Isolation on High Speed Channels   | See Fig. 2 for Measurement Setup   | f = 2.7 GHz | -21                 | -19  |      |
|  |  |  | f = 3.0 GHz | -21                 | -19  |      |
| I <sub>LOSS</sub>  | Differential Insertion Loss on High speed channels                                       | @5.4Gbps (see figure 3, Vcom = 0V)   | -1.8        | -1.6                |      | dB   |
| I <sub>LOSS</sub>  | Differential Insertion Loss on High Speed HDMI Channels                                  | @6Gbps (see figure 3, Vcom = 3.0V)   |             | -2.5                |      | dB   |
| R <sub>loss</sub>  | Differential Return Loss on High speed channels  | @ 2.7GHz (5.4Gbps)   |             | -18                 | -15  | dB   |
| BW_Dx±   | Bandwidth -3dB for Main High speed path (Dx±)  | See figure 3   | 5.0         | 5.4                 |      | GHz  |
| BW_Dx±   | Bandwidth -3dB for Main high speed HDMI path (Dx±)                                       | See figure 3   | 4.7         | 5.0                 |      | GHz  |
| BW_AUX   | Bandwidth -3dB for AUX   | See figure 3   | 1.2         | 1.5                 |      | GHz  |
| T <sub>sw a-b</sub>  | time it takes to switch from port A to port B  | Manual selection   |             |                     | 1    | us   |
| T <sub>sw b-a</sub>  | time it takes to switch from port B to port A  | Manual selection   |             |                     | 1    | us   |
| T <sub>startup</sub>   | Vdd valid to channel enable  | Manual selection   |             |                     | 10   | us   |
| T <sub>wakeup</sub>  | Enabling output by changing OEB from High to Low   | Manual selection   |             |                     | 10   | us   |



**Fig 1. Crosstalk Setup**

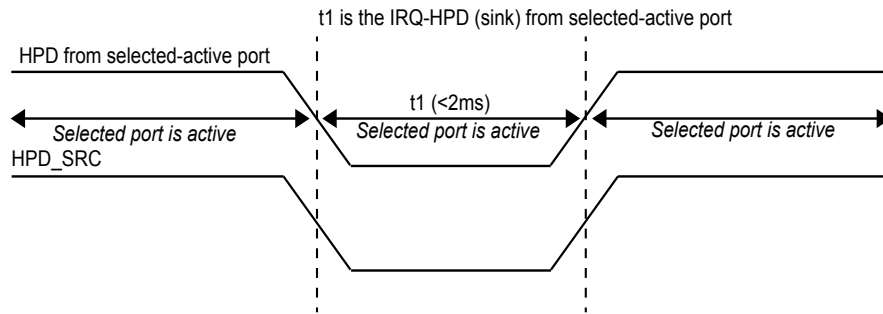


**Fig 2. Off-isolation setup**

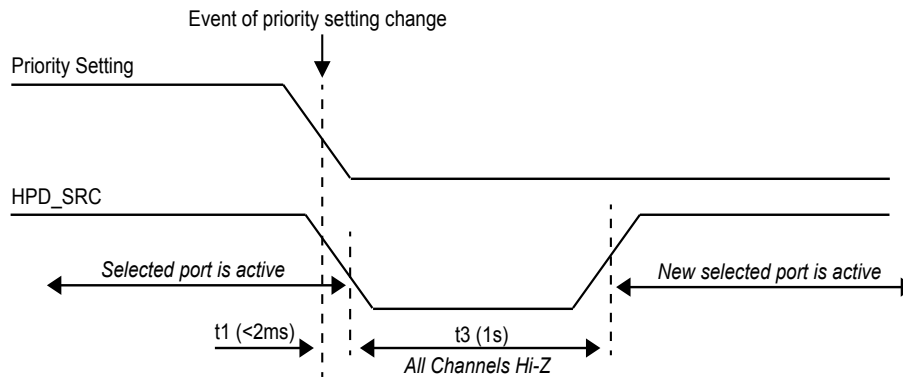


**Fig 3. Differential Insertion Loss**

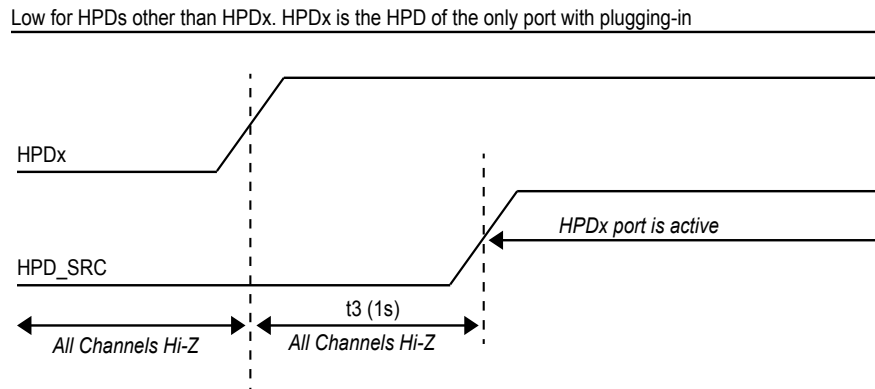
**HPD timing waveform (DEMUX mode)**



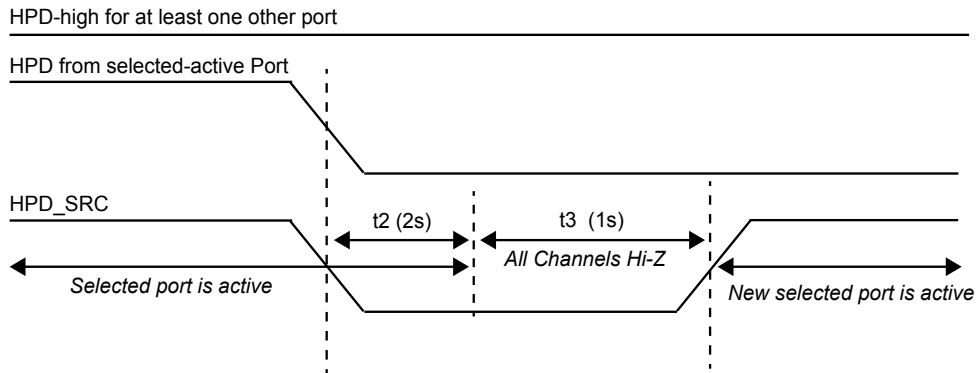
**Fig 4. HPD timing t1. HPD\_SRC low and the active of selected port will follow t1, if t1 further extended less than t2 (125ms) when auto switch and manual switch**



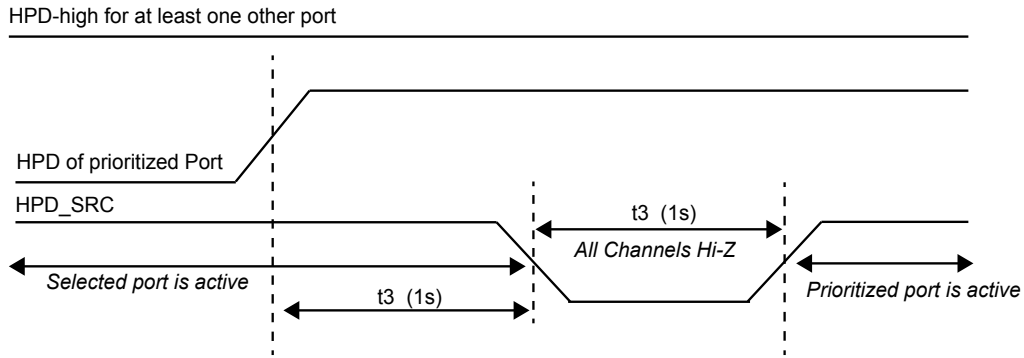
**Fig 5. HPD timing t3. All channels” include DP-HDMI data, AUX, DDC, HPD and CAB\_DET when auto switch**



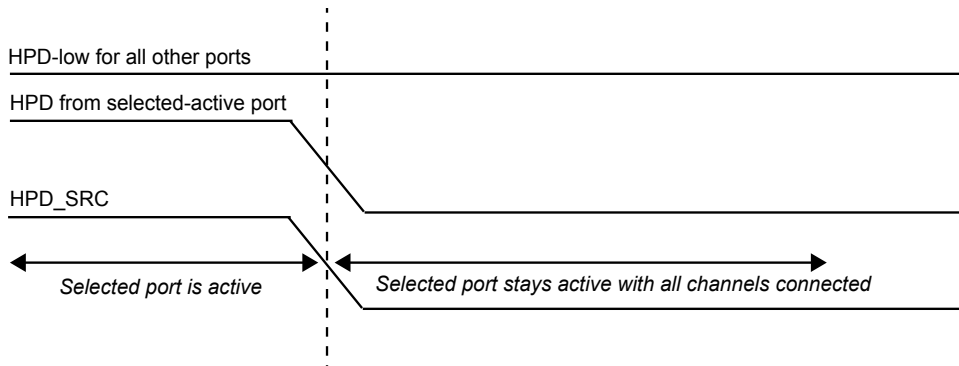
**Fig 6. HPD timing t3 when auto switch**



**Fig 7. HPD timing when auto switch**

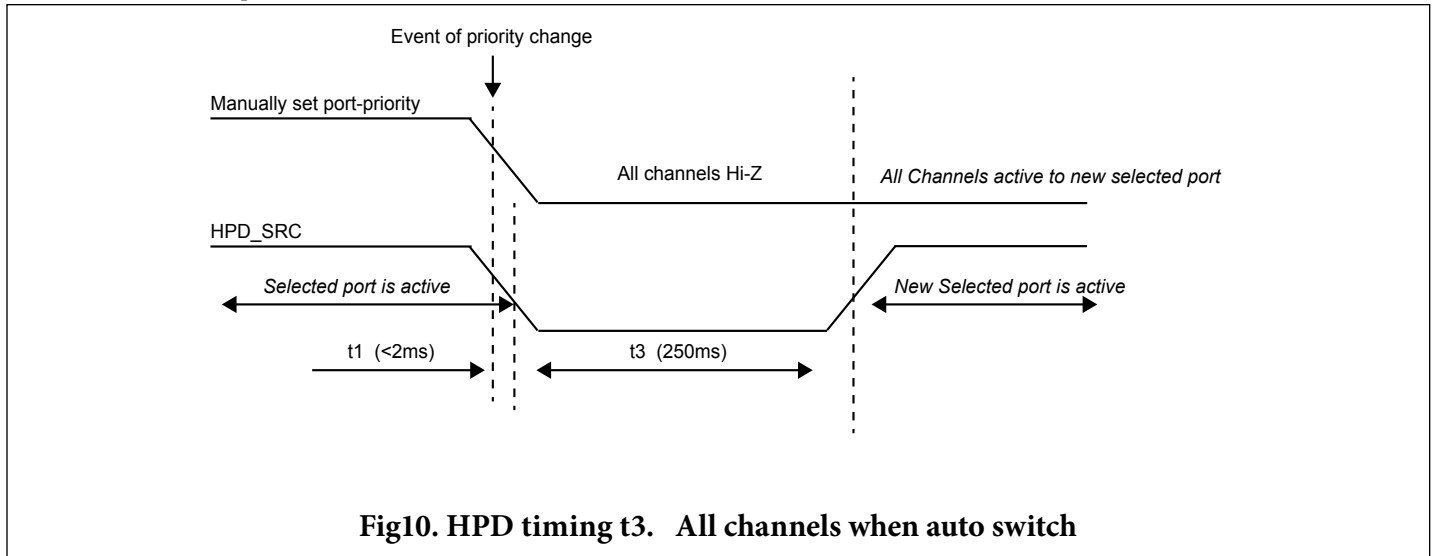


**Fig 8. HPD timing when auto switch**



**Fig 9. HPD timing when auto switch and manual switch**

**Port Selection by Manual Mode**



| Parameter  | Test Conditions | Min. | Typ.* | Max. | Unit |
|--|-----------------|------|-------|------|------|
| <b>HPD auto switching timing</b>   |                 |      |       |      |      |
| HPD pulse duration when treated as an IRQ -t1 (Figure 4)                       |                 |      |       | 2    | ms   |
| Propagation delay of HPDx Desertion -t2 (Figure 7)                             |                 | 1.2s | 2s    | 3s   | s    |
| HPD_SRC low duration when the outputs are switched -t3(Figure 5, 6, 7, 8, 10); |                 | 0.6s | 1s    | 1.5s | s    |
| Propagation delay of HPDx assertion (Figure 8)                                 |                 |      |       |      |      |

**PI3WVR31310A**

**Packaging Mechanical: ZL60**

| SYMBOLS | MIN.       | NOM. | MAX. |
|---------|------------|------|------|
| A       | 0.70       | 0.75 | 0.80 |
| A1      | 0.00       | 0.02 | 0.05 |
| A3      | 0.203 REF. |      |      |
| b       | 0.15       | 0.20 | 0.25 |
| D       | 4.90       | 5.00 | 5.10 |
| E       | 8.90       | 9.00 | 9.10 |
| e       | 0.40 BSC   |      |      |
| L       | 0.30       | 0.40 | 0.50 |
| D2      | 2.90       | 3.00 | 3.10 |
| E2      | 6.90       | 7.00 | 7.10 |

**NOTE :**

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220.
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

|  |                |
|--|----------------|
| <b>PERICOM</b><br>Enabling Serial Connectivity | DATE: 04/08/14 |
| DESCRIPTION: 60-Pin, TQFN 5X9mm                |                |
| PACKAGE CODE: ZL (ZL60)                        |                |
| DOCUMENT CONTROL #: PD-2182                    | REVISION: -    |

14-0044

Note: For latest package info, please check: <http://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/>

**Ordering Information**

| Ordering Code    | Package Code | Package Description               |
|------------------|--------------|-----------------------------------|
| PI3WVR31310AZLE  | ZL           | 60-Pin, (TQFN) 5X9mm              |
| PI3WVR31310AZLEX | ZL           | 60-Pin, (TQFN) 5X9mm, Tape & Reel |

**Notes:**

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging



**IMPORTANT NOTICE**

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and definitive format released by Diodes Incorporated.

**LIFE SUPPORT**

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or

2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

Copyright © 2016, Diodes Incorporated

[www.diodes.com](http://www.diodes.com)

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Diodes Incorporated:](#)

[PI3WVR31310AZLEX](#)